Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

Claims 1-93 (canceled)

94. (previously presented) A semiconductor chip or wafer comprising:

a silicon substrate;

a first metallization structure over said silicon substrate;

a passivation layer over said first metallization structure; and

a second metallization structure over said passivation layer, wherein said second metallization structure comprises a metal layer having a thickness of between 2 and 100 μm, and wherein said second metallization structure connects multiple separate portions of said first metallization structure.

95. (previously presented) The semiconductor chip or wafer of claim 94, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip or wafer.

96. (previously presented) The semiconductor chip or wafer of claim 94, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

97. (previously presented) The semiconductor chip or wafer of claim 94, wherein said passivation layer comprises a topmost CVD-formed layer of said semiconductor chip or wafer.

98. (previously presented) The semiconductor chip or wafer of claim 94, wherein said first metallization structure comprises a first contact pad exposed by an opening in said passivation layer, and said second metallization structure comprises a second contact pad connected to said first contact pad, wherein the positions of said first and second contact pads from a top view are different.

99. (previously presented) The semiconductor chip or wafer of claim 94, wherein said metal layer comprises gold.

100. (previously presented) The semiconductor chip or wafer of claim 99, wherein said second metallization structure further comprises an underlying metal layer under said metal layer, wherein said underlying metal layer comprises titanium tungsten.

Claim 101 (canceled)

102. (previously presented) The semiconductor chip or wafer of claim 94 further comprising a topmost polymer layer over said passivation layer, wherein said second metallization structure is over said topmost polymer layer.

Claims 103 and 104 (canceled)

105. (previously presented) The semiconductor chip or wafer of claim 94, wherein said metal layer is electroplated.

106. (previously presented) A semiconductor chip or wafer comprising:

a silicon substrate;

a first metallization structure over said silicon substrate, wherein said first metallization structure comprises a first contact pad;

a passivation layer over said first metallization structure, wherein an opening in said passivation layer exposes said first contact pad; and

a second metallization structure over said passivation layer, wherein said second metallization structure comprises a gold layer with a thickness of between 2 and 100 μm, wherein said second metallization structure comprises a second contact pad connected to said first contact pad, and wherein the positions of said first and second contact pads from a top view are different.

107. (previously presented) The semiconductor chip or wafer of claim 106, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip or wafer.

108. (previously presented) The semiconductor chip or wafer of claim 106, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

109. (previously presented) The semiconductor chip or wafer of claim 106, wherein said passivation layer comprises a topmost CVD-formed layer of said semiconductor chip or wafer.

110. (previously presented) The semiconductor chip or wafer of claim 106, wherein said second metallization structure further comprises a metal layer under said gold layer, wherein said metal layer comprises titanium tungsten.

Claim 111 (canceled)

112. (previously presented) The semiconductor chip or wafer of claim 106, wherein said second contact pad is used to be wirebonded thereto.

113. (previously presented) The semiconductor chip or wafer of claim 106 further comprising a wirebond on said second contact pad.

114. (previously presented) The semiconductor chip or wafer of claim 106 further comprising a metal bump on said second contact pad.

115. (previously presented) The semiconductor chip or wafer of claim 106 further comprising a solder bump on said second contact pad..

116. (previously presented) The semiconductor chip or wafer of claim 106 further comprising a topmost polymer layer over said passivation layer, wherein said gold layer is over said topmost polymer layer.

Claims 117 and 118 (canceled)

119. (previously presented) The semiconductor chip or wafer of claim 106, wherein said gold layer is electroplated.

120. (currently amended) A semiconductor chip or wafer comprising:

a silicon substrate;

a first metallization structure over said silicon substrate, wherein said first metallization structure comprises a first contact pad;

a passivation layer over said first metallization structure, wherein an opening in said passivation layer exposes a top surface of said first contact pad; and

a second contact pad connected to said top surface. ~~first contact pad,~~ wherein said second contact pad comprises a gold layer with a thickness of between 2 and 100 μm and wherein said second contact pad is used to be wirebonded thereto.

Claims 121 and 122 (canceled)

123. (previously presented) The semiconductor chip or wafer of claim 120 further comprising a polymer layer over said passivation layer, wherein said second contact pad is over said polymer layer.

Claims 124 and 125 (canceled)

126. (previously presented) The semiconductor chip or wafer of claim 120, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip or wafer.

127. (previously presented) The semiconductor chip or wafer of claim 120, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

128. (previously presented) The semiconductor chip or wafer of claim 120, wherein said passivation layer comprises a topmost CVD-formed layer of said semiconductor chip or wafer.

129. (previously presented) The semiconductor chip or wafer of claim 120, wherein said gold layer is electroplated.

Claim 130 (canceled)

131. (previously presented) The semiconductor chip or wafer of claim 120 further comprising a wirebond on said second contact pad.

Claims 132-135 (canceled)